



IEEE

IEC 61523-1

Edition 2.0 2012-06

INTERNATIONAL STANDARD

IEEE Std 1481™

**Delay and power calculation standards –
Part 1: Integrated circuit delay and power calculation systems**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE **XH**

ICS 25.040; 35.060

ISBN 978-2-83220-107-7

Warning! Make sure that you obtained this publication from an authorized distributor.

Contents

1	Overview.....	1
1.1	Scope.....	1
1.2	Purpose.....	2
1.3	Introduction.....	2
2	Normative references.....	3
3	Definitions.....	4
4	Acronyms and abbreviations.....	13
5	Typographical conventions.....	14
5.1	Syntactic elements.....	14
5.2	Conventions.....	15
6	DPCS flow.....	16
6.1	Overview.....	16
6.1.1	Procedural interface.....	17
6.1.2	Global policies and conventions.....	17
6.2	Flow of control.....	17
6.3	DPCM—application relationships.....	18
6.3.1	Technology library.....	18
6.3.2	Subrule.....	18
6.4	Interoperability.....	18
7	Delay calculation language (DCL).....	19
7.1	Character set.....	19
7.2	Lexical elements.....	19
7.2.1	Whitespace.....	19
7.2.2	Comments.....	19
7.2.3	Tokens.....	19
7.2.4	Header names.....	31
7.2.5	Preprocessing directives.....	31
7.3	Context.....	31
7.3.1	Space.....	31
7.3.2	Plane.....	31
7.3.3	Context operation.....	31
7.3.4	Library parallelism.....	31
7.3.5	Application parallelism.....	32
7.4	Data types.....	32
7.4.1	Base types.....	32
7.4.2	Native data types.....	32
7.4.3	Mathematical calculation data types.....	32
7.4.4	Pointer data types.....	33
7.4.5	Aggregate data types.....	33
7.5	Identifiers.....	39
7.5.1	Name spaces of identifiers.....	39
7.5.2	Storage durations of objects.....	39
7.5.3	Scope of identifiers.....	40
7.5.4	Linkages of identifiers.....	41
7.6	Operator descriptions.....	41
7.6.1	String prefix operator.....	41
7.6.2	Explicit string prefix operator.....	41
7.6.3	Embedded string prefix operator.....	42
7.6.4	String prefix semantics.....	42
7.6.5	Assignment operator.....	42
7.6.6	New operator.....	42
7.6.7	SCOPE operator(s).....	43

7.6.8	Launch operator.....	44
7.6.9	Purity operator.....	44
7.6.10	Force operator.....	45
7.7	Timing propagation.....	45
7.7.1	Timing checks.....	46
7.7.2	Test mode operators.....	46
7.8	Expressions.....	48
7.8.1	Array subscripting.....	49
7.8.2	Statement calls.....	49
7.8.3	General syntax.....	49
7.8.4	Method statement calls.....	49
7.8.5	Assign variable reference.....	50
7.8.6	Store variable reference.....	50
7.8.7	Mathematical expressions.....	50
7.8.8	Mathematical operators.....	51
7.8.9	Discrete math expression.....	52
7.8.10	INT discrete.....	52
7.8.11	PINLIST discrete.....	53
7.8.12	Logical expressions and operators.....	53
7.8.13	MODE expressions.....	53
7.8.14	Embedded C code expressions.....	55
7.8.15	Computation order.....	56
7.9	DCL mathematical statements.....	58
7.9.1	Statement names.....	58
7.9.2	Clauses.....	58
7.9.3	Modifiers.....	62
7.9.4	Prototypes.....	64
7.9.5	Statement failure.....	67
7.9.6	Type definition statements.....	67
7.9.7	Interfacing statements.....	68
7.9.8	DCL to C communication.....	70
7.9.9	Constant statement.....	71
7.9.10	Calculation statements.....	71
7.9.11	METHOD statement.....	74
7.10	Predefined types.....	75
7.10.1	ACTIVITY_HISTORY_TYPE.....	75
7.10.2	HISTORY_TYPE.....	76
7.10.3	LOAD_HISTORY_TYPE.....	77
7.10.4	CELL_LIST_TYPE.....	77
7.10.5	TECH_TYPE.....	78
7.10.6	DELAY_REC_TYPE.....	78
7.10.7	SLEW_REC_TYPE.....	78
7.10.8	CHECK_REC_TYPE.....	78
7.10.9	CCDB_TYPE.....	79
7.10.10	CELL_DATA_TYPE.....	79
7.10.11	PCDB_TYPE.....	79
7.10.12	PIN_ASSOCIATION.....	79
7.10.13	PATH_DATA_TYPE.....	80
7.10.14	STD STRUCT.....	80
7.11	Predefined variables.....	80
7.11.1	ARGV.....	80
7.11.2	CONTROL_PARM.....	81
7.12	Built-in function calls.....	81
7.12.1	ABS.....	81
7.12.2	Complex number components.....	81
7.12.3	EXPAND.....	82

7.12.4	Array functions.....	82
7.12.5	Messaging functions.....	82
7.13	Tables.....	84
7.13.1	TABLEDEF statement.....	85
7.13.2	Table visibility rules.....	87
7.13.3	TABLE statement.....	87
7.13.4	LOAD_TABLE statement.....	91
7.13.5	UNLOAD_TABLE statement.....	93
7.13.6	WRITE_TABLE statement.....	94
7.13.7	ADD_ROW statement.....	94
7.13.8	DELETE_ROW statement.....	95
7.14	Built-in library functions.....	96
7.14.1	Numeric conversion functions.....	96
7.14.2	Tech_family functions.....	98
7.14.3	Trigonometric functions.....	99
7.14.4	Context manipulation functions.....	99
7.14.5	Debug controls.....	101
7.14.6	Utility functions.....	102
7.14.7	Table functions.....	102
7.14.8	Subrule controls.....	103
7.15	Library control statements.....	104
7.15.1	Meta-variables.....	105
7.15.2	TECH_FAMILY.....	105
7.15.3	RULENAME.....	105
7.15.4	CONTROL_PARM.....	105
7.15.5	SUBRULE statement.....	105
7.15.6	Path list expansion rules.....	106
7.15.7	SUBRULES statement.....	107
7.15.8	Control file.....	107
7.15.9	TECH_FAMILY statement.....	109
7.15.10	SUBRULE and SUBRULES statements.....	109
7.16	Modeling.....	110
7.16.1	Types of modeling.....	110
7.16.2	Model organization.....	111
7.16.3	MODELPROC statement.....	112
7.16.4	SUBMODEL statement.....	113
7.16.5	Modeling statements.....	114
7.16.6	TEST_BUS statement.....	124
7.16.7	INPUT statement.....	124
7.16.8	OUTPUT statement.....	128
7.16.9	DO statement.....	129
7.16.10	PROPERTIES statement.....	153
7.16.11	SETVAR statement.....	154
7.17	Embedded C code.....	155
7.18	Definition of a subrule.....	155
7.19	Pragma.....	156
7.19.1	IMPORT_EXPORT_TAG.....	156
8	Power modeling and calculation.....	157
8.1	Power overview.....	157
8.2	Caching state information.....	158
8.2.1	Initializing the state cache.....	158
8.2.2	State cache lifetime.....	158
8.3	Caching load and slew information.....	158
8.3.1	Loading the load and slew cache.....	159
8.3.2	Load and slew cache lifetime.....	159

8.4	Simulation switching events.....	159
8.5	Partial swing events.....	160
8.6	Power calculation.....	160
8.7	Accumulation of power consumption by the design.....	162
8.8	Group Pin List syntax and semantics.....	162
8.8.1	Syntax.....	162
8.8.2	Semantics.....	162
8.8.3	Example.....	163
8.9	Group Condition List syntax and semantics.....	163
8.9.1	Syntax.....	163
8.9.2	Semantics.....	163
8.9.3	Example.....	164
8.10	Sensitivity list syntax and semantics.....	164
8.10.1	Syntax.....	164
8.10.2	Semantics.....	164
8.10.3	Example.....	165
8.11	Group condition language.....	165
8.11.1	Syntax.....	165
8.11.2	Semantics.....	166
8.11.3	Condition expression operator precedence.....	168
8.11.4	Condition expressions referencing pin states and transitions.....	168
8.11.5	Semantics of nonexistent pins.....	168
9	Application and library interaction.....	170
9.1	behavior model domain.....	170
9.2	vectorTiming and vectorPower model domains.....	170
9.2.1	Power unit conversion.....	170
9.2.2	Vector power calculation.....	171
10	Procedural interface (PI).....	172
10.1	Overview.....	172
10.1.1	DPCM.....	172
10.1.2	Application.....	172
10.1.3	libdcmr.....	172
10.2	Control and data flow.....	173
10.3	Architectural requirements.....	173
10.4	Data ownership technique.....	173
10.4.1	Persistence of data passed across the PI.....	173
10.4.1	Data cache guidelines for the DPCM.....	174
10.4.2	Application/DPCM interaction.....	174
10.4.3	Application initializes message/memory handling.....	174
10.4.4	Application loads and initializes the DPCM.....	174
10.4.5	Application requests timing models for cell instances.....	175
10.5	Model domain issues.....	175
10.5.1	Model domain selection.....	175
10.5.2	Model domain determination.....	175
10.5.3	DPCM invokes application modeling callback functions.....	175
10.5.4	Application requests propagation delay.....	176
10.5.5	DPCM calls application EXTERNAL functions.....	177
10.6	Reentry requirements.....	177
10.7	Application responsibilities when using a DPCM.....	177
10.7.1	Standard Structure rules.....	177
10.7.2	User object registration.....	177
10.7.3	Selection of early and late slew values.....	178
10.7.4	Semantics of slew values.....	178
10.7.5	Slew calculations.....	179

10.8	Application use of the DPCM.....	179
10.8.1	Initialization of the DPCM.....	179
10.8.2	Context creation.....	180
10.8.3	Dynamic linking.....	180
10.8.4	Subrule initialization.....	181
10.8.5	Use of the DPCM.....	181
10.8.6	Application control.....	181
10.8.7	Application execution.....	182
10.8.8	Termination of DPCM.....	182
10.9	DPCM library organization.....	182
10.9.1	Multiple technologies.....	182
10.9.2	Model names.....	183
10.9.3	DPCM error handling.....	183
10.10	C level language for EXPOSE and EXTERNAL functions.....	183
10.10.1	Integer return code.....	183
10.10.2	The Standard Structure pointer.....	184
10.10.3	Result structure pointer.....	184
10.10.4	Passed arguments.....	184
10.10.5	DCL array indexing.....	184
10.10.6	Conversion to C data types.....	184
10.10.7	include files.....	185
10.11	PIN and BLOCK data structure requirements.....	186
10.12	DCM_STD_STRUCT Standard Structure.....	186
10.12.1	Alternate semantics for Standard Structure fields.....	189
10.12.2	Reserved fields.....	190
10.12.3	Standard Structure value restriction.....	190
10.13	DCMTransmittedInfo structure.....	190
10.14	Environment or user variables.....	190
10.15	Procedural interface (PI) functions summary.....	190
10.15.1	Expose functions.....	191
10.15.2	External functions.....	199
10.15.3	Deprecated functions.....	202
10.16	Implicit functions.....	205
10.16.1	libdcmr.....	205
10.16.2	Run-time library utility functions.....	206
10.16.3	Memory control functions.....	206
10.16.4	Message and error control functions.....	208
10.16.5	Calculation functions.....	208
10.16.6	Modeling functions.....	208
10.17	PI function table description.....	209
10.17.1	Arguments.....	209
10.17.2	DCL syntax.....	210
10.17.3	C syntax.....	210
10.18	PI function descriptions.....	210
10.18.1	Interconnect loading related functions.....	210
10.18.2	Interconnect delay related functions.....	217
10.18.3	Functions accessing netlist information.....	221
10.18.4	Functions exporting limit information.....	229
10.18.5	Functions getting/setting model information.....	231
10.18.6	Functions importing instance name information.....	244
10.18.7	Process information functions.....	246
10.18.8	Miscellaneous standard interface functions.....	247
10.18.9	Power-related functions.....	257
10.19	Application context.....	265
10.19.1	pathData association.....	265

10.20	Application and library interaction.....	265
10.20.1	behavior model domain.....	266
10.20.2	vectorTiming and vectorPower model domains.....	267
10.20.3	Power unit conversion.....	267
10.20.4	Vector power calculation.....	267
10.21	Parasitic analysis.....	268
10.21.1	Assumptions.....	268
10.21.2	Parasitic networks.....	268
10.21.3	Basic definitions.....	268
10.21.4	Parasitic element data structure.....	270
10.21.5	Coordinates.....	274
10.21.6	Parasitic subnets.....	274
10.21.7	Pin parasitics.....	282
10.21.8	Modeling internal nodes.....	285
10.21.9	Load and interconnect models.....	287
10.21.10	Obtaining parasitic networks.....	291
10.21.11	Persistent storage of load and interconnect models.....	292
10.21.12	Calculating effective capacitances and driving resistances.....	295
10.21.13	Parasitic estimation.....	298
10.21.14	Threshold voltages.....	303
10.21.15	Obtaining aggressor window overlaps.....	304
10.22	Noise analysis.....	311
10.22.1	Types of noise.....	312
10.22.2	Noise models.....	313
10.22.3	Noise waveforms.....	315
10.22.4	Noise network models.....	322
10.22.5	Calculating composite noise at cell inputs.....	327
10.22.6	Calculating composite noise at cell outputs.....	330
10.22.7	Setting noise budgets.....	334
10.22.8	Reporting noise violations.....	335
10.23	Delay and slew calculations for differential circuits.....	338
10.23.1	Sample figures.....	338
10.23.2	appGetArrivalOffsetsByName.....	339
10.23.3	API extensions for function modeling.....	340
10.23.4	Explicit APIs for user-defined primitives.....	348
10.23.5	APIs for hierarchy.....	350
10.23.6	Built-in APIs for function modeling.....	350
10.23.7	API Extensions for VECTOR modeling.....	351
10.23.8	APIs for XWF.....	352
10.23.9	Extensions and changes to voltages and temperature APIs.....	356
10.23.10	Operating conditions.....	358
10.23.11	On-chip process variation.....	360
10.23.12	Accessing properties and attributes.....	367
10.23.13	APIs for attribute within a PIN object.....	387
10.23.14	Connectivity.....	395
10.23.15	Control of timing arc existence and state.....	397
10.23.16	Modeling cores.....	402
10.23.17	Default pin slews and interface version calls.....	407
10.23.18	API to access library required resources.....	408
10.23.19	Resource types.....	410
10.23.20	Library extensions for phase locked loop processing.....	411
10.23.21	API definitions for external conditions.....	412
10.23.22	Extensions for listing pins.....	416
10.23.23	Memory BIST mapping.....	417
10.23.24	dpcmGetCellTestProcedure.....	419

10.24	Interconnect delay calculation intraface.....	419
10.24.1	Control and data flows.....	420
10.24.2	Model generation functions.....	421
10.24.3	Calculation functions.....	423
10.24.4	Cell calculation functions.....	424
10.24.5	ICM initialization.....	429
10.25	DCL run-time support.....	435
10.25.1	Array manipulation functions.....	435
10.25.2	Memory management.....	438
10.25.3	Structure manipulation functions.....	439
10.25.4	Initialization functions.....	443
10.26	Calculation functions.....	455
10.26.1	delay.....	455
10.26.2	slew.....	456
10.26.3	check.....	457
10.27	Modeling functions.....	459
10.27.1	modelSearch.....	459
10.27.2	Mode operators.....	461
10.27.3	Arrival time merging.....	462
10.27.4	Edge propagation communication to the application.....	462
10.27.5	Edge propagation communication to the DPCM.....	466
10.27.6	newTimingPin.....	466
10.27.7	newDelayMatrixRow.....	467
10.27.8	newNetSinkPropagateSegments.....	468
10.27.9	newNetSourcePropagateSegments.....	470
10.27.10	newPropagateSegment.....	471
10.27.11	newTestMatrixRow.....	471
10.27.12	newAltTestSegment.....	472
10.27.13	Interactions between interconnect modeling and modeling functions.....	473
10.28	Deprecated functions.....	473
10.28.1	Parasitic handling.....	474
10.28.2	Array manipulation functions.....	482
10.28.3	Memory management.....	484
10.28.4	Initialization functions.....	487
10.29	Standard Structure (std_stru.h) file.....	499
10.30	Standard macros (std_mac.h) file.....	519
10.31	Standard interface structures (dcmintf.h) file.....	527
10.32	Standard loading (dcmload.h) file.....	531
10.33	Standard debug (dcmdebug.h) file.....	534
10.34	Standard array (dcmgarray.h) file.....	561
10.35	Standard user array defines (dcmuarray.h) file.....	566
10.36	Standard platform-dependency (dcmpltfm.h) file.....	570
10.37	Standard state variables (dcmstate.h) file.....	576
11	Parasitics.....	580
11.1	Introduction.....	580
11.2	Targeted applications for SPEF.....	580
11.3	SPEF specification.....	580
11.3.1	Grammar.....	580
11.3.2	Escaping rules.....	582
11.3.3	File syntax.....	583
11.3.4	Comments.....	589
11.3.5	File semantics.....	589
11.4	Examples.....	609
11.4.1	Basic *D_NET file.....	609
11.4.2	Basic *R_NET file.....	612
11.4.3	*R_NET with poles and residues plus name mapping.....	613

11.4.4	*D_NET with triplet par_value.....	615
11.4.5	*R_NET with poles and residues plus triplet par_value.....	618
11.4.6	Merging SPEF files.....	619
11.4.7	A SPEF file header section with *VARIATION_PARAMETERS definition.....	624
11.4.8	CAP and RES statements with sensitivity information in a SPEF file.....	624
Annex A	(normative) Implementation requirements.....	625
Annex B	(informative) IEEE List of Participants.....	629

Table of Tables

Table 1—Keywords.....	20
Table 2—DCL predefined references to Standard Structure fields.....	23
Table 3—DCL compiler generated predefined identifiers.....	27
Table 4—Edge types and conversions	29
Table 5—Propagation mode conversions.....	29
Table 6—Calculation mode conversions.....	29
Table 7—TEST_TYPE conversions.....	30
Table 8—Purity operator.....	45
Table 9—Timing resolution modes.....	45
Table 10—Test mode operators table.....	46
Table 11—Mathematical operators.....	51
Table 12—Logical operators.....	53
Table 13—Mathematical operator precedence (high to low).....	56
Table 14—Logical operator precedence (high to low).....	56
Table 15—Type definition for ACTIVE_HISTORY_TYPE.....	75
Table 16—Permitted activityCode values.....	76
Table 17—Type definition for HISTORY_TYPE.....	76
Table 18—Rule history info message types.....	76
Table 19—Table History inform message types	77
Table 20—Permitted kind values.....	77
Table 21—LOAD_HISTORY TYPE.....	77
Table 22—CELL_LIST_TYPE.....	78
Table 23—TECH_TYPE.....	78
Table 24—DELAY_REC_TYPE	78
Table 25—SLEW_REC_TYPE	78
Table 26—CHECK_REC_TYPE.....	79
Table 27—CCDB_TYPE.....	79
Table 28—CELL_DATA_TYPE.....	79
Table 29—CCDB_TYPE	79
Table 30—PIN_ASSOCIATION	80
Table 31—PATH_DATA_TYPE.....	80
Table 32—STD_STRUCT.....	80
Table 33—ARGV.....	81
Table 34—CONTROL_PARM.....	81
Table 35—Library function floor.....	96
Table 36—Library function ifloor	97
Table 37—Library function ceil.....	97
Table 38—Library Function iceil.....	97
Table 39—Library function rint.....	97
Table 40—Library function round	97
Table 41—Library function trunc	98
Table 42—Library function itrunc	98
Table 43—Library function map_tech_family	98
Table 44—Library function current_tech_type	98
Table 45—Library function subrule_tech_type	98
Table 46—Library function subrule_tech_type.....	99
Table 47—Library function get_technology_list.....	99
Table 48—Library function cos.....	99
Table 49—Library function sin	99
Table 50—Library function tan	99
Table 51—Library function new_plane	100
Table 52—Library function get_plane_name	100
Table 53—Library function get_space_name.....	100

Table 54—Library function <code>get_max_spaces</code>	100
Table 55—Library function <code>get_max_planes</code>	100
Table 56—Library function <code>get_space_coordinate</code>	101
Table 57—Library function <code>get_plane_coordinate</code>	101
Table 58—Library function <code>set_busy_wait</code>	101
Table 59—Library function <code>change_debug_level</code>	102
Table 60—Library function <code>get_caller_stack</code>	102
Table 61—Library function <code>GET_LOAD_HISTORY</code>	102
Table 62—Library function <code>GET_CELL_LIST</code>	102
Table 63—Library function <code>GET_ROW_COUNT</code>	103
Table 64—Library function <code>STEP_TABLE</code>	103
Table 65—Library function <code>GET_LOAD_PATH</code>	103
Table 66—Library function <code>GET_RULE_NAME</code>	104
Table 67—Library function <code>ADD_RULE</code>	104
Table 68—Data type clause.....	118
Table 69—Arc data types.....	119
Table 70—Validity of predefined identifiers for <code>STORE</code> clause.....	128
Table 71—Logic operators (valid for behavior, vectorTiming, and vectorPower model domains).....	133
Table 72—Logical equivalence operators (valid for behavior model domain).....	134
Table 73—Unary bitwise operators (valid for behavior, vectorTiming, and vectorPower model domains)	134
Table 74—Binary bitwise operators (valid for behavior, vectorTiming, and vectorPower model domains)	134
Table 75—Binary operators (valid for behavior model domain).....	134
Table 76—Node primitives for control operators (valid for behavior model domain).....	135
Table 77—Node primitives for edge operators (continued) (valid for behavior, vectorTiming, and vectorPower model domains).....	135
Table 78—Node primitives for precedence control operators (valid for behavior model domain).....	136
Table 79—Node primitives for constant operators (valid for behavior, vectorTiming, vectorPower model domains).....	136
Table 80—Node primitives for user-defined operators.....	136
Table 81—Node primitives for miscellaneous operators.....	137
Table 82—Binary reduction operators.....	138
Table 83—Bitwise reduction operators	139
Table 84—Logical reduction operators.....	140
Table 85—Array of bits operators.....	141
Table 86—Edge operators.....	142
Table 87—Higher function nodes.....	143
Table 88—Constant value nodes.....	146
Table 89—Miscellaneous operators	146
Table 90—User-defined operators.....	147
Table 91—Valid modifier enumerations for given node primitive operators.....	148
Table 92—Syntax for a <code>GroupPinString</code>	162
Table 93—Syntax for a <code>GroupConditionString</code>	163
Table 94—Syntax for a <code>SensitivityPinString</code>	164
Table 95—Syntax for a <code>condition_expression</code>	165
Table 96— <code>PinName_Identifier</code> semantics	167
Table 97— <code>PinName_Level</code> semantics.....	167
Table 98— <code>PinName_State</code> semantics.....	167
Table 99—Condition expression operators.....	168
Table 100—Interaction between multiple technologies and application.....	183
Table 101—Return code most significant byte.....	183
Table 102—Return code least significant bytes.....	184
Table 103—Data types defined in DCL and C.....	184
Table 104—Header files.....	185
Table 105—Predefined macro names.....	186

Table 106—Alternate semantics for Standard Structure fields.....	189
Table 107—Expose functions.....	191
Table 108—External functions.....	199
Table 109—Deprecated functions.....	203
Table 110—libdcmr functions.....	205
Table 111—Module control functions.....	206
Table 112—Memory control functions.....	207
Table 113—Message and error control functions.....	208
Table 114—Calculation functions.....	208
Table 115—Modeling functions.....	209
Table 116—PI function table example.....	209
Table 117—Standard Structure field semantics.....	210
Table 118—appGetTotalLoadCapacitanceByPin.....	211
Table 119—appGetTotalLoadCapacitanceByName.....	211
Table 120—appGetTotalPinCapacitanceByPin.....	212
Table 121—appGetTotalPinCapacitanceByName.....	212
Table 122—appGetSourcePinCapacitanceByPin.....	213
Table 123—appGetSourcePinCapacitanceByName.....	213
Table 124—dpcmGetDefCellSize.....	214
Table 125—appGetCellCoordinates.....	214
Table 126—appGetCellOrientation.....	215
Table 127—dpcmGetEstLoadCapacitance.....	215
Table 128—dpcmGetEstWireCapacitance.....	216
Table 129—dpcmGetEstWireResistance.....	216
Table 130—dpcmGetPinCapacitance.....	217
Table 131—dpcmGetCellIOLists.....	217
Table 132—appGetRC.....	218
Table 133—dpcmGetDelayGradient.....	219
Table 134—dpcmGetSlewGradient.....	219
Table 135—dpcmGetEstimateRC.....	220
Table 136—dpcmGetDefPortSlew.....	220
Table 137—dpcmGetDefPortCapacitance.....	221
Table 138—appGetNumDriversByPin.....	221
Table 139—appGetNumDriversByName.....	222
Table 140—appForEachParallelDriverByPin.....	222
Table 141—appForEachParallelDriverByName.....	224
Table 142—appGetNumPinsByPin.....	225
Table 143—appGetNumPinsByName.....	225
Table 144—appGetNumSinksByPin.....	226
Table 145—appGetNumSinksByName.....	226
Table 146—dpcmAddWireLoadModel.....	227
Table 147—dpcmGetWireLoadModel.....	228
Table 148—dpcmGetWireLoadModelForBlockSize.....	229
Table 149—appGetInstanceCount.....	229
Table 150—dpcmGetCapacitanceLimit.....	230
Table 151—dpcmGetSlewLimit.....	230
Table 152—dpcmGetXovers.....	231
Table 153—dpcmGetFunctionalModeArray.....	231
Table 154—dpcmGetBaseFunctionalMode.....	232
Table 155—appGetCurrentFunctionalMode.....	233
Table 156—dpcmGetControlExistence.....	233
Table 157—dpcmSetLevel.....	234
Table 158—dpcmGetLibraryAccuracyLevelArrays.....	235
Table 159—dpcmSetLibraryAccuracyLevel.....	236
Table 160—dpcmGetExposePurityAndConsistency.....	236
Table 161—DCM_Purity.....	237

Table 162—DCM_Consistency.....	237
Table 163—dpcmGetRailVoltageArray.....	237
Table 164—dpcmGetBaseRailVoltage.....	238
Table 165—appGetCurrentRailVoltage.....	238
Table 166—dpcmGetWireLoadModelArray.....	239
Table 167—dpcmGetBaseWireLoadModel.....	239
Table 168—appGetCurrentWireLoadModel.....	240
Table 169—dpcmGetBaseTemperature.....	240
Table 170—dpcmGetBaseOpRange.....	241
Table 171—dpcmGetOpRangeArray.....	241
Table 172—appGetCurrentTemperature.....	242
Table 173—appGetCurrentOpRange.....	242
Table 174—dpcmGetTimingStateArray.....	243
Table 175—appGetCurrentTimingState.....	244
Table 176—dpcmGetCellList.....	244
Table 177—appGetCellName.....	245
Table 178—appGetHierPinName.....	245
Table 179—appGetHierBlockName.....	246
Table 180—appGetHierNetName.....	246
Table 181—dpcmGetThresholds.....	246
Table 182—appGetThresholds.....	247
Table 183—appGetExternalStatus.....	248
Table 184—appGetVersionInfo.....	248
Table 185—appGetResource.....	249
Table 186—dpcmGetRuleUnitToSeconds.....	249
Table 187—dpcmGetRuleUnitToOhms.....	249
Table 188—dpcmGetRuleUnitToFarads.....	250
Table 189—dpcmGetRuleUnitToHenries.....	251
Table 190—dpcmGetRuleUnitToWatts.....	251
Table 191—dpcmGetRuleUnitToJoules.....	252
Table 192—dpcmGetTimeResolution.....	252
Table 193—dpcmGetParasiticCoordinateTypes.....	253
Table 194—dpcmIsSlewTime.....	253
Table 195—dpcmDebug.....	254
Table 196—dpcmGetVersionInfo.....	254
Table 197—dpcmHoldControl.....	255
Table 198—dpcmFillPinCache.....	255
Table 199—dpcmFreePinCache.....	256
Table 200—appRegisterCellInfo.....	256
Table 201—dpcmGetCellPowerInfo.....	257
Table 202—dpcmGetCellPowerWithState.....	258
Table 203—dpcmGetAETCellPowerWithSensitivity.....	259
Table 204—Integer LSB example.....	259
Table 205—Mask encoding.....	259
Table 206—dpcmGetPinPower.....	260
Table 207—dpcmAETGetSettlingTime.....	260
Table 208—dpcmAETGetSimultaneousSwitchTime.....	261
Table 209—dpcmGroupGetSettlingTime.....	261
Table 210—dpcmGroupGetSimultaneousSwitchTime.....	262
Table 211—dpcmCalcPartialSwingEnergy.....	262
Table 212—dpcmSetInitialState.....	263
Table 213—dpcmFreeStateCache.....	264
Table 214—appGetStateCache.....	264
Table 215—dpcmGetNetEnergy.....	265
Table 216—parasiticElement structure.....	270
Table 217—Parasitic element variables.....	271

Table 218—DCM_ElementTypes.....	271
Table 219—Node variables.....	272
Table 220—Value variables.....	272
Table 221—Coordinate structure.....	274
Table 222—parasiticSubnet structure.....	274
Table 223—DCM_NodeTypes.....	275
Table 224—dpcmCreateSubnetStructure.....	279
Table 225—dpcmGetDefaultInterconnectTechnology.....	281
Table 226—dpcmScaleParasitics.....	281
Table 227—dpcmGetSinkPinParasitics.....	284
Table 228—dpcmGetSourcePinParasitics.....	284
Table 229—dpcmGetPortNames.....	285
Table 230—Application timing arcs.....	287
Table 231—dpcmBuildLoadModels.....	288
Table 232—dpcmBuildInterconnectModels.....	289
Table 233—appGetInterconnectModels.....	290
Table 234—appGetLoadModels.....	290
Table 235—appGetParasiticNetworksByPin.....	291
Table 236—appGetParasiticNetworksByName.....	292
Table 237—dpcmPassivateLoadModels.....	293
Table 238—dpcmPassivateInterconnectModels.....	293
Table 239—dpcmRestoreLoadModels.....	294
Table 240—dpcmRestoreInterconnectModels.....	294
Table 241—appGetCeff.....	295
Table 242—dpcmCalcCeff.....	296
Table 243—dpcmCalcSteadyStateResistanceRange.....	296
Table 244—dpcmCalcTristateResistanceRange.....	297
Table 245—appSetCeff.....	298
Table 246—dpcmCalcCouplingCapacitance.....	300
Table 247—dpcmCalcSubstrateCapacitance.....	300
Table 248—dpcmCalcSegmentResistance.....	301
Table 249—Manufacturing layer type values.....	301
Table 250—dpcmGetLayerArray.....	302
Table 251—dpcmGetRuleUnitToMeters.....	302
Table 252—dpcmGetRuleUnitToAmps.....	303
Table 253—appGetDriverThresholds.....	303
Table 254—appGetAggressorOverlapWindows.....	305
Table 255—appSetAggressorInteractWindows.....	307
Table 256—appGetOverlapNWFs.....	308
Table 257—appSetDriverInteractWindows.....	309
Table 258—dpcmCalcOutputResistances.....	310
Table 259—DCM_NoiseTypes.....	312
Table 260—docmGetLibraryNoiseTypesArray.....	312
Table 261—appNewNoiseCone.....	314
Table 262—NWF type.....	316
Table 263—PWF type.....	317
Table 264—PWFdriverModel.....	318
Table 265—dpcmGetPWFarray.....	318
Table 266—dpcmCreatePWF.....	319
Table 267—dpcmCopyNWFarray.....	320
Table 268—dpcmCopyPWF.....	320
Table 269—dpcmCreatePWFdriverModel.....	321
Table 270—dpcmGetPWFdriverModelArray.....	321
Table 271—dpcmGetSinkPinNoiseParasitics.....	324
Table 272—dpcmGetSourcePinNoiseParasitics.....	325
Table 273—dpcmBuildNoiseInterconnectModels.....	325

Table 274—dpcmBuildNoiseLoadModels.....	326
Table 275—driverPinNoise.....	328
Table 276—dpcmCalcInputNoise.....	329
Table 277—relatedPinNoise.....	331
Table 278—dpcmCalcOutputNoise.....	332
Table 279—appForEachNoiseParallelDriver.....	333
Table 280—dpcmSetParallelRelatedNoise.....	334
Table 281—appSetParallelOutputNoise.....	334
Table 282—dpcmSetNoiseLimit.....	335
Table 283—noiseViolationInfo.....	335
Table 284—appSetNoiseViolation.....	337
Table 285—dpcmGetNoiseViolationDetails.....	337
Table 286—appGetArrivalOffsetsByName.....	339
Table 287—appGetArrivalOffsetArraysByName.....	340
Table 288—Arc ordering.....	343
Table 289—PathDataBlock->modifiers enumeration values for priority operation.....	343
Table 290—DCM_TestTypes.....	348
Table 291—dpcmPerformPrimitive.....	348
Table 292—appGetArcStructure.....	349
Table 293—dpcmGetNodeSensitivity.....	349
Table 294—dpcmModelMoreFunctionDetail.....	350
Table 295—XWF APIs.....	353
Table 296—appSetXWF.....	354
Table 297—appGetXWF.....	355
Table 298—dpcmCalcXWF.....	356
Table 299—dpcmGetCellRailVoltageArray.....	356
Table 300—dpcmGetBaseCellRailVoltageArray.....	357
Table 301—dpcmGetBaseCellTemperature.....	358
Table 302—dpcmGetOpPointArray.....	359
Table 303—dpcmGetBaseOpPoint.....	359
Table 304—dpcmSetCurrentOpPoint.....	360
Table 305—DCM_ProcessVariations.....	361
Table 306—New predefined identifiers.....	362
Table 307—DCM_CalculationModes.....	363
Table 308—dpcmSetCurrentProcessPoint.....	363
Table 309—dpcmGetBaseProcessPoint.....	364
Table 310—dpcmGetProcessPointRange.....	364
Table 311—dpcmGetRailVoltageRangeArray.....	365
Table 312—dpcmGetCellRailVoltageRangeArray.....	366
Table 313—dpcmGetTemperatureRange.....	366
Table 314—dpcmGetCellTemperatureRange.....	367
Table 315—dpcmGetPinPinTypeArray.....	368
Table 316—dpcmGetPinPinType.....	369
Table 317—dpcmGetPinSignalTypeArray.....	369
Table 318—dpcmGetPinSignalType.....	371
Table 319—dpcmGetPinActionArray.....	371
Table 320—dpcmGetPinAction.....	372
Table 321—dpcmGetPinPolarityArray.....	372
Table 322—dpcmGetPinPolarity.....	373
Table 323—dpcmGetPinEnablePin.....	373
Table 324—dpcmGetPinConnectClass.....	374
Table 325—dpcmGetPinScanPosition.....	374
Table 326—dpcmGetPinStuckArray.....	375
Table 327—dpcmGetPinStuck.....	375
Table 328—dpcmGetDifferentialPairPin.....	376
Table 329—dpcmGetPathLabel.....	376

Table 330—dpcmGetPowerStateLabel.....	377
Table 331—dpcmGetCellTypeArray.....	377
Table 332—dpcmGetCellType.....	379
Table 333—dpcmGetCellSwapClassArray.....	379
Table 334—dpcmGetCellSwapClass.....	380
Table 335—dpcmGetCellRestrictClassArray.....	381
Table 336—dpcmGetCellRestrictClass.....	382
Table 337—dpcmGetCellScanTypeArray.....	382
Table 338—dpcmGetCellScanType.....	383
Table 339—dpcmGetCellNonScanCell.....	383
Table 340—DCM_PinMappingTypes.....	385
Table 341—appSetVectorOperations.....	385
Table 342—DCM_VectorOperations.....	386
Table 343—dpcmGetLevelShifter.....	386
Table 344—dpcmGetPinTiePolarity.....	387
Table 345—dpcmGetPinReadPolarity.....	388
Table 346—dpcmGetPinWritePolarity.....	388
Table 347—dpcmGetSimultaneousSwitchTimes.....	388
Table 348—appGetSwitchingBits.....	389
Table 349—dpcmGetFrequencyLimit.....	390
Table 350—appGetPinFrequency.....	390
Table 351—dpcmGetBasePinFrequency.....	391
Table 352—dpcmGetPinJitter.....	391
Table 353—dpcmGetInductanceLimit.....	392
Table 354—dpcmGetOutputSourceResistances.....	392
Table 355—appSetPull.....	393
Table 356—DCM_PullType.....	393
Table 357—dpcmGetPull.....	393
Table 358—dpcmGetPinDriveStrength.....	394
Table 359—dpcmGetCellVectorPower.....	395
Table 360—dpcmGetPinConnectivityArrays.....	395
Table 361—dpcmGetLibraryConnectClassArray.....	396
Table 362—dpcmGetLibraryConnectivityRules.....	396
Table 363—DCM_ConnectRules.....	397
Table 364—dpcmGetExistenceGraph.....	398
Table 365—dpcmGetTimingStateGraphs.....	399
Table 366—dpcmGetTimingStateStrings.....	401
Table 367—dpcmGetVectorEdgeNumbers.....	402
Table 368—appSetSignalDivision.....	403
Table 369—appSetSignalMultiplication.....	404
Table 370—appSetSignalGeneration.....	406
Table 371—dpcmGetDefPinSlews.....	407
Table 372—appGetInterfaceVersion.....	408
Table 373—Valid interface version strings.....	408
Table 374—dpcmSetResource.....	409
Table 375—dpcmGetAllResources.....	409
Table 376—DCM_ResourceTypes.....	410
Table 377—appGetExternalDelayByPin.....	412
Table 378—Description of multiArcMultiEdgePath (XXXX are do not care bits).....	413
Table 379—appGetExternalDelayByName.....	414
Table 380—appGetLogicLevelByName.....	415
Table 381—DCM_LogicLevel.....	415
Table 382—appGetLogicLevelByPin.....	416
Table 383—dpcmGetPinIndexArrays.....	416
Table 384—dpcmGetSupplyPins.....	417
Table 385—DCM_BistInversion.....	418

Table 386—dpcmGetPhysicalBISTMap.....	418
Table 387—dpcmGetLogicalBISTMap.....	418
Table 388—dpcmGetCellTestProcedure.....	419
Table 389—icmBuildLoadModels.....	422
Table 390—icmBuildInterconnectModels.....	422
Table 391—icmCalcInterconnectDelaySlew.....	423
Table 392—icmCalcCellDelaySlew.....	424
Table 393—ccmCalcDelaySlew.....	425
Table 394—ccmEarlyLateIdentical.....	426
Table 395—ccmGetICMcontrolParams.....	427
Table 396—icmCalcOutputResistances.....	427
Table 397—icmCalcTotalLoadCapacitances.....	428
Table 398—icmCalcXWF.....	429
Table 399—icmInit.....	429
Table 400—dcmRT_new_DCM_ARRAY.....	435
Table 401—DCM_ATYPE enumeration.....	436
Table 402—DCM_AINIT enumeration.....	436
Table 403—DCM_ArrayInitUserFunction.....	437
Table 404—dcmRT_sizeof_DCM_ARRAY.....	437
Table 405—dcmRT_claim_DCM_ARRAY.....	438
Table 406—dcmRT_disclaim_DCM_ARRAY.....	438
Table 407—dcmRT_disclaim_DCM_STRUCT.....	439
Table 408—dcmRT_disclaim_DCM_STRUCT.....	440
Table 409—dcmRT_longlock_DCM_STRUCT.....	440
Table 410—dcmRT_longunlock_DCM_STRUCT.....	441
Table 411—dcmRT_getNumDimensions.....	442
Table 412—dcmRT_getNumElementsPer.....	442
Table 413—dcmRT_getNumElements.....	442
Table 414—dcmRT_getElementType.....	443
Table 415—dcmRT_arraycmp.....	443
Table 416—dcmRT_InitRuleSystem.....	444
Table 417—dcmRT_BindRule.....	445
Table 418—dcmRT_AppendRule.....	446
Table 419—dcmRT_UnbindRule.....	447
Table 420—dcmRT_FindFunction.....	448
Table 421—dcmRT_FindAppFunction.....	448
Table 422—dcmRT_QuietFindFunction.....	449
Table 423—dcmRT_MakeRC.....	449
Table 424—dcmRT_HardErrorRC.....	450
Table 425—dcmRT_SetMessageIntercept.....	450
Table 426—dcmRT_IssueMessage.....	451
Table 427—dcmRT_new_DCM_STD_STRUCT.....	451
Table 428—dcmRT_delete_DCM_STD_STRUCT.....	452
Table 429—dcmRT_setTechnology.....	452
Table 430—dcmRT_getTechnology.....	453
Table 431—dcmRT_getAllTechs.....	453
Table 432—dcmRT_freeAllTechs.....	453
Table 433—dcmRT_isGeneric.....	454
Table 434—dcmRT_takeMappingOfNugget.....	454
Table 435—dcmRT_registerUserObject.....	454
Table 436—dcmRT_DeleteRegisteredUserObjects.....	455
Table 437—dcmRT_DeleteOneUserObject.....	455
Table 438—delay.....	456
Table 439—slew.....	456
Table 440—check.....	457
Table 441—modelSearch.....	459

Table 442—Mode propagation operators.....	461
Table 443—Mode computation operators for delay and slew.....	461
Table 444—Mode operator enumerators for check.....	462
Table 445—Edge propagation enumeration pairs.....	463
Table 446—Edge propagation communication with DPCM.....	466
Table 447—newTimingPin.....	467
Table 448—newDelayMatrixRow.....	467
Table 449—newNetSinkPropagateSegments.....	468
Table 450—newNetSourcePropagateSegments.....	470
Table 451—newPropagateSegment.....	471
Table 452—newTestMatrixRow.....	472
Table 453—newAltTestSegment.....	472
Table 454—appGetPiModel.....	474
Table 455—appGetPolesAndResidues.....	475
Table 456—appGetCeffective.....	476
Table 457—appGetRLCnetworkByPin.....	476
Table 458—appGetRLCnetworkByName.....	477
Table 459—dpcmCalcPiModel.....	478
Table 460—dpcmCalcPolesAndResidues.....	478
Table 461—dpcmCalcCeffective.....	479
Table 462—dpcmSetRLCmember.....	480
Table 463—dpcmAppendPinAdmittance.....	481
Table 464—dpcmDeleteRLCnetwork.....	482
Table 465—dcm_copy_DCM_ARRAY.....	483
Table 466—dcm_new_DCM_ARRAY.....	483
Table 467—dcm_sizeof_DCM_ARRAY.....	483
Table 468—dcm_lock_DCM_ARRAY.....	484
Table 469—dcm_unlock_DCM_ARRAY.....	484
Table 470—dcm_lock_DCM_STRUCT.....	485
Table 471—dcm_unlock_DCM_STRUCT.....	485
Table 472—dcm_getNumDimensions.....	485
Table 473—dcm_getNumElementsPer.....	486
Table 474—dcm_getNumElements.....	486
Table 475—dcm_getElementType.....	486
Table 476—dcm_arraycmp.....	487
Table 477—dcmCellList.....	487
Table 478—dcmSetNewStorageManager.....	488
Table 479—dcmMalloc.....	488
Table 480—dcmFree.....	489
Table 481—dcmRealloc.....	489
Table 482—dcmBindRule.....	489
Table 483—dcmAddRule.....	490
Table 484—dcmUnbindRule.....	490
Table 485—dcmFindFunction.....	490
Table 486—dcmFindAppFunction.....	491
Table 487—dcmQuietFindFunction.....	491
Table 488—dcmMakeRC.....	492
Table 489—dcmHardErrorRC.....	492
Table 490—dcmSetMessageIntercept.....	492
Table 491—dcmIssueMessage.....	493
Table 492—dcm_rule_init.....	493
Table 493—DCM_new_DCM_STD_STRUCT.....	494
Table 494—DCM_delete_DCM_STD_STRUCT.....	495
Table 495—dcm_setTechnology.....	495
Table 496—dcm_getTechnology.....	496
Table 497—dcm_getAllTechs.....	496

Table 498—dcm_freeAllTechs.....	496
Table 499—dcm_isGeneric.....	497
Table 500—dcm_mapNugget.....	497
Table 501—dcm_takeMappingOfNugget.....	498
Table 502—dcm_registerUserObject.....	498
Table 503—dcm_DeleteRegisteredUserObjects.....	498
Table 504—dcm_DeleteOneUserObject.....	499
Table 505—Design flow values.....	591
Table 506—conn_attr.....	595
Table 507—Variation effect equations.....	598

Table of BNF Syntax

Syntax 7.1: token.....	19
Syntax 7.2: identifier.....	22
Syntax 7.3: double_quoted_character.....	23
Syntax 7.4: constant.....	28
Syntax 7.5: string_literal.....	30
Syntax 7.6: operator.....	30
Syntax 7.7: punctuator.....	30
Syntax 7.8: native_type.....	32
Syntax 7.9: mathematical_type.....	33
Syntax 7.10: pointer_data_type.....	33
Syntax 7.11: aggregate_type.....	34
Syntax 7.12: aggregate_access.....	34
Syntax 7.13: array_type.....	36
Syntax 7.14: var.....	37
Syntax 7.15: cast.....	39
Syntax 7.16: new_operator.....	42
Syntax 7.17: scope_change.....	44
Syntax 7.18: launch.....	44
Syntax 7.19: FORCE operator.....	45
Syntax 7.20: array_index.....	49
Syntax 7.21: statement_call.....	49
Syntax 7.22: method_statement_call.....	50
Syntax 7.23: assign_variable_reference.....	50
Syntax 7.24: store_variable_reference.....	50
Syntax 7.25: expression.....	51
Syntax 7.26: discrete_expression.....	52
Syntax 7.27: logical_expression.....	53
Syntax 7.28: pin_range_list.....	54
Syntax 7.29: c_statement_reference.....	55
Syntax 7.30: passed_clause.....	58
Syntax 7.31: result_prototype.....	59
Syntax 7.32: conditional_result.....	60
Syntax 7.33: local_clause.....	61
Syntax 7.34: default_clause.....	62
Syntax 7.35: default_clause (result variable).....	62
Syntax 7.36: prototype_modifier.....	65
Syntax 7.37: common_prototype.....	65
Syntax 7.38: tabledef_prototype.....	66
Syntax 7.39: load_table_prototype.....	66
Syntax 7.40: add_row_prototype.....	66
Syntax 7.41: delay_prototype.....	67
Syntax 7.42: check_prototype.....	67
Syntax 7.43: submodel_prototype.....	67
Syntax 7.44: typedef.....	68
Syntax 7.45: expose_statement.....	68
Syntax 7.46: external_statement.....	69
Syntax 7.47: internal_statement.....	70
Syntax 7.48: constant_statement.....	71
Syntax 7.49: calculation_body.....	71
Syntax 7.50: calc_statement.....	71
Syntax 7.51: assign_statement.....	72
Syntax 7.52: delay_statement.....	72
Syntax 7.53: slew_statement.....	73

Syntax 7.54: check_statement.....	74
Syntax 7.55: check_statement.....	74
Syntax 7.56: ABS.....	81
Syntax 7.57: IMAG_PART.....	81
Syntax 7.58: REAL_PART.....	82
Syntax 7.59: EXPAND.....	82
Syntax 7.60: IS_EMPTY.....	82
Syntax 7.61: NUM_DIMENSIONS.....	82
Syntax 7.62: NUM_ELEMENTS.....	82
Syntax 7.63: ISSUE_MESSAGE.....	83
Syntax 7.64: PRINT_VALUE.....	84
Syntax 7.65: SOURCE_STRANDS_MSB.....	84
Syntax 7.66: SOURCE_STRANDS_LSB.....	84
Syntax 7.67: SINK_STRANDS_MSB.....	84
Syntax 7.68: SINK_STRANDS_LSB.....	84
Syntax 7.69: tabledef_statement.....	85
Syntax 7.70: table_statement.....	88
Syntax 7.71: load_table_statement.....	91
Syntax 7.72: unload_table_statement.....	93
Syntax 7.73: unload_table_statement.....	94
Syntax 7.74: add_row_statement.....	94
Syntax 7.75: delete_row_statement.....	95
Syntax 7.76: subrule_statement.....	105
Syntax 7.77: subrules_statement.....	107
Syntax 7.78: tech_family_statement.....	109
Syntax 7.79: tech_family_statement.....	111
Syntax 7.80: model_procedure.....	112
Syntax 7.81: submodel_procedure.....	113
Syntax 7.82: path_separator_stmt.....	114
Syntax 7.83: path_statement.....	115
Syntax 7.84: path_list.....	116
Syntax 7.85: clkflg_clause.....	117
Syntax 7.86: ckttype_clause.....	118
Syntax 7.87: object_type_clause.....	118
Syntax 7.88: data_type_sequence.....	118
Syntax 7.89: bus_statement.....	120
Syntax 7.90: test_statement.....	121
Syntax 7.91: compare_list.....	121
Syntax 7.92: compare_clause.....	121
Syntax 7.93: edges_clause.....	122
Syntax 7.94: test_type_clause.....	122
Syntax 7.95: cycleadj_clause.....	123
Syntax 7.96: checks_clause.....	123
Syntax 7.97: methods_list.....	123
Syntax 7.98: store_clause.....	124
Syntax 7.99: test_bus_statement.....	124
Syntax 7.100: input_statement.....	125
Syntax 7.101: methods_clause.....	125
Syntax 7.102: store_clause.....	126
Syntax 7.103: output_statement.....	128
Syntax 7.104: do_statement – BREAK and CONTINUE.....	130
Syntax 7.105: do_statement.....	131
Syntax 7.106: statement_reference.....	131
Syntax 7.107: statement_reference.....	132
Syntax 7.108: node_sequence.....	132
Syntax 7.109: function_assignment_expression.....	151

Syntax 7.110: vector_sequence.....	152
Syntax 7.111: import_export_sequence.....	153
Syntax 7.112: properties_statement.....	154
Syntax 7.113: setvar_statement.....	154
Syntax 7.114: embedded_C_code.....	155
Syntax 7.115: subrule.....	155
Syntax 7.116: pragma_declare.....	156
Syntax 11.1: Alphanumeric characters.....	581
Syntax 11.2: SPEF names.....	582
Syntax 11.3: SPEF_file.....	583
Syntax 11.4: header_def.....	583
Syntax 11.5: unit_def.....	584
Syntax 11.6: name_map.....	584
Syntax 11.7: power_def.....	584
Syntax 11.8: external_def.....	585
Syntax 11.9: conn_attr.....	585
Syntax 11.10: define_def.....	585
Syntax 11.11: variation_def.....	586
Syntax 11.12: internal_def.....	586
Syntax 11.13: d_net.....	586
Syntax 11.14: conn_sec.....	587
Syntax 11.15: cap_sec.....	587
Syntax 11.16: res_sec.....	587
Syntax 11.17: induc_sec.....	587
Syntax 11.18: r_net.....	588
Syntax 11.19: load_desc.....	588
Syntax 11.20: d_pnet.....	588
Syntax 11.21: pconn_sec.....	588
Syntax 11.22: pcap_sec.....	589
Syntax 11.23: pres_sec.....	589
Syntax 11.24: pinduc_sec.....	589
Syntax 11.25: r_pnet.....	589

Table of Figures

Figure 1—High-level DPCS architecture linkage structure.....	16
Figure 2—Function graph form.....	110
Figure 3—DPCM/application procedural interface.....	173
Figure 4—PIN and PINLIST.....	186
Figure 5—Parallel drivers example.....	223
Figure 6—Subnet node mapping.....	278
Figure 7—Differential buffer chain.....	338
Figure 8—Timing models for a differential buffer chain	338
Figure 9—Arrival offsets for differential signals	338
Figure 10—Priority operation.....	344
Figure 11—Precedence.....	345
Figure 12—Strand ranges	346
Figure 13—Various methods of using XWF to model waveforms for slew computation	352
Figure 14—Propagation of XWF “handles” by application.....	353
Figure 15—Application, CCM and ICM control and data flows.....	421
Figure 16—Clock separation.....	458
Figure 17—Bias calculation.....	458
Figure 18—Clock pulse width.....	459
Figure 19—Sample MODELPROC results.....	469
Figure 20—Additional MODELPROC results.....	470
Figure 21—Capacitance value example.....	474
Figure 22—Equation for poles and residues.....	475
Figure 23—Example RC network.....	481
Figure 24—SPEF targeted applications.....	580

Delay and power calculation standards -

Part 1: Integrated circuit delay and power calculation systems

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation.

IEEE Standards documents are developed within IEEE Societies and Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. IEEE develops its standards through a consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of IEEE and serve without compensation. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards. Use of IEEE Standards documents is wholly voluntary. IEEE documents are made available for use subject to important notices and legal disclaimers (see <http://standards.ieee.org/IPR/disclaimers.html> for more information).

IEC collaborates closely with IEEE in accordance with conditions determined by agreement between the two organizations.

- 2) The formal decisions of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees. The formal decisions of IEEE on technical matters, once consensus within IEEE Societies and Standards Coordinating Committees has been reached, is determined by a balanced ballot of materially interested parties who indicate interest in reviewing the proposed standard. Final approval of the IEEE standards document is given by the IEEE Standards Association (IEEE-SA) Standards Board.
- 3) IEC/IEEE Publications have the form of recommendations for international use and are accepted by IEC National Committees/IEEE Societies in that sense. While all reasonable efforts are made to ensure that the technical content of IEC/IEEE Publications is accurate, IEC or IEEE cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications (including IEC/IEEE Publications) transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC/IEEE Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC and IEEE do not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC and IEEE are not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or IEEE or their directors, employees, servants or agents including individual experts and members of technical committees and IEC National Committees, or volunteers of IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board, for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC/IEEE Publication or any other IEC or IEEE Publications.
- 8) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that implementation of this IEC/IEEE Publication may require use of material covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. IEC or IEEE shall not be held responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patent Claims or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility.

International Standard IEC 61523-1/ IEEE Std 1481-2009 has been processed through IEC technical committee 93: Design automation, under the IEC/IEEE Dual Logo Agreement.

This second edition cancels and replaces the first edition, published in 2001, and constitutes a technical revision.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
IEEE Std 1481-2009	93/318/FDIS	93/325/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The IEC Technical Committee and IEEE Technical Committee have decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IEEE Std 1481™-2009
(Revision of
IEEE Std 1481-1999)

IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)

Sponsor

Design Automation Standards Committee

of the

IEEE Computer Society

9 December 2009

IEEE-SA Standards Board

Royalty-free nonexclusive permission has been granted by International Business Machines (IBM) Corporation for all written contributions made by IBM under the direction of Harry J. Beatty III.

Royalty-free permission has been granted by Silicon Integration Initiative, Inc. (Si2) to reprint material from Specification for the Open Library Architecture (OLA), Version 2.0-00, March 1, 2003.

Abstract: Ways for integrated circuit designers to analyze chip timing and power consistently across a broad set of electric design automation (EDA) applications are covered in this standard. Methods by which integrated circuit vendors can express timing and power information once per given technology are also covered. In addition, the means by which EDA vendors can meet their application performance and capacity needs are discussed.

Keywords: chip delay, electronic design automation (EDA), integrated circuit (IC) design, power calculation

IEEE Introduction

This introduction is not part of IEEE Std 1481-2009, IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA).

The objective of the delay and power calculation system (DPCS) is to make it possible for integrated circuit designers to consistently calculate chip delay and power across electronic design automation (EDA) applications and for integrated circuit vendors to express delay and power information only once per technology while enabling sufficient EDA application accuracy.

This is accomplished by a coordinated set of standards that support a standard method to describe timing and power characteristics of integrated circuit design units (cells and higher level design elements); a standard method for EDA applications to calculate chip design instance specific delay, slew, and power for logic and interconnects; and standard file formats to exchange chip parasitic and cluster information.

Notice to users

Laws and regulations

Users of these documents should consult all applicable laws and regulations. Compliance with the provisions of this standard does not imply compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Copyrights

This document is copyrighted by the IEEE. It is made available for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making this document available for use and adoption by public authorities and private users, the IEEE does not waive any rights in copyright to this document.

Updating of IEEE documents

Users of IEEE standards should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect. In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit the IEEE Standards Association Web site at <http://ieeexplore.ieee.org/xpl/standards.jsp>, or contact the IEEE at the address listed previously.

For more information about the IEEE Standards Association or the IEEE standards development process, visit the IEEE-SA Web site at <http://standards.ieee.org>.

Errata

Errata, if any, for this and all other standards can be accessed at the following URL: <http://standards.ieee.org/reading/ieee/updates/errata/>. Users are encouraged to check this URL for errata periodically.

Interpretations

Current interpretations can be accessed at the following URL: <http://standards.ieee.org/reading/ieee/interp/>.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. A patent holder or patent applicant has filed a statement of assurance that it will grant licenses under these rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses. Other Essential Patent Claims may exist for which a statement of assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions are reasonable or non-discriminatory. Further information may be obtained from the IEEE Standards Association.

Delay and power calculation standards – Part 1: Integrated circuit delay and power calculation systems

IMPORTANT NOTICE: This trial-use standard is not intended to ensure safety, security, health, or environmental protection in all circumstances. Implementers of the trial-use standard are responsible for determining appropriate safety, security, environmental, and health practices or regulatory requirements.

This IEEE document is made available for use subject to important notices and legal disclaimers. These notices and disclaimers appear in all publications containing this document and may be found under the heading “Important Notice” or “Important Notices and Disclaimers Concerning IEEE Documents.” They can also be obtained on request from IEEE or viewed at <http://standards.ieee.org/IPR/disclaimers.html>.

1 Overview

The delay and power calculation system (DPCS) is a coordinated set of standards that support a standard method to describe timing and power characteristics of integrated circuit (IC) design units (cells and higher level design elements); a standard method for electronic design automation (EDA) applications to calculate chip design instance specific delay, slew, and power for logic and interconnects; and standard file formats to exchange chip parasitic and cluster information. The standard specifications covered in this document include

- A description language for timing and power modeling, called the delay calculation language (DCL).
- A software procedural interface (PI) for communications between EDA applications and compiled libraries of DCL descriptions.
- A standard file exchange format for parasitic information about the chip design: Standard Parasitic Exchange Format (SPEF).
- Informative usage examples
- Informative notes

Notes and examples are informative. All other components of this specification are considered normative unless otherwise directed.

1.1 Scope

The scope of this standard focuses on delay and power calculation for integrated circuit design with support for modeling logical behavior and signal integrity.

1.2 Purpose

To improve the IEEE 1481-1999 standard system for integrated circuit designers to more accurately and more completely analyze semiconductor designs across EDA applications and for integrated circuit vendors to express logical behavior, signal integrity, delay, and power information only once per technology while enabling sufficient EDA application accuracy.

1.3 Introduction

The DPCS standard covers delay and power calculation for integrated circuit design with support for modeling logical behavior and signal integrity, which makes it possible for integrated circuit designers to analyze chip timing and power consistently across a broad set of EDA applications, for integrated circuit vendors to express timing and power information once (for a given technology), and for EDA vendors to meet their application performance and capacity needs. The intended use for this standard is IC timing and power. This standard may be applied to both unit logic cells supplied by the IC vendor and logical macros defined by the IC designer. Although this standard is written toward the integrated circuit supplier and EDA developer, its application applies equally well to representation of timing and power for designer-defined macros (or hierarchical design elements).

These specifications make it possible to achieve consistent timing and power results, but they do not guarantee it. They provide for a single executable software program that computes delay and power based on IC vendor-supplied algorithms (or designer-supplied algorithms for macros) but does not guarantee EDA applications can correctly communicate the design-specific information required for these algorithms. By specifying standard exchange formats for parasitic data and floorplanning information, this standard provides a marked improvement over design environments with no such standards. However, it is the responsibility of the EDA application to correctly correlate the information between these standard exchange files and the actual design. This standard also does not detail how the information contained within the standard exchange files shall be obtained.

As feature sizes for chips have shrink below 0.25 μm , interconnect delay effects have begun to outweigh those of the logic cells. This means placement of cells and wire routing of the interconnects become as important a factor as the type of cell drivers and receivers on the interconnect. As a result, EDA logic design applications (such as synthesis) have begun to interact closely with physical design applications (such as floorplanning and layout). Applications that before could consider only simple delay and power models now need to deal with complex, interrelated delay and power algorithms. Plus, due to the complexities of the delay and power algorithms, the integrated circuit vendor needs to have control of application calculations and not be restricted by the limitations of a broad set of applications demanded by the customers (the designers).

Over the past few years, it has become increasingly apparent that modern very large-scale integration (VLSI) design is no longer bounded only by timing and area constraints. Power has become significantly more important. In an era of hand-held devices, ranging from mobile computing to wireless communication systems, managing and controlling power takes on an important role. Several benefits can be attained from low-power designs in addition to extended battery life. Low-power devices often run at a lower junction temperature, which leads to higher reliability and lower cost cooling systems. There are also several challenges for calculation and modeling of power (and delay) in deep submicron (less than 0.25 μm) designs. EDA tools can now accurately calculate and model power by using this DPCS standard.

2 Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

ISO/IEC 9899:1990, Programming Languages – C.¹

ISO/IEC 14882:2003, Programming Languages – C++.

¹ ISO publications are available from the ISO Central Secretariat, Case Postale 56, 1 ch. de la Voie Creuse, CH-1211, Genève 20, Switzerland / Suisse (<http://www.iso.ch/>). IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3 rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse (<http://www.iec.ch/>).